INCH POUND

MIL-PRF-32192
w/ Amendment 4
12 July 2022
SUPERSEDING
MIL-PRF-32192
w/ Amendment 3
10 July 2017

PERFORMANCE SPECIFICATION

RESISTOR, CHIP, THERMAL (THERMISTOR),
GENERAL SPECIFICATION FOR

This specification is approved for use by all Departments
and Agencies of the Department of Defense.

1. SCOPE

1.1 Scope. This specification covers the general requirements for fixed, chip, thermal resistors. These thermistors exhibit a positive temperature coefficient (PTC) or a negative temperature coefficient (NTC) and are primarily intended for incorporation into surface mount applications. These devices are to be used for temperature control, temperature compensation, sensing, and frequency compensation over the temperature range specified.

1.2 Classification.

1.2.1 Part or Identification Number (PIN). The PIN is in the following form and as specified (see 3.1 and 6.2).

M32192	A	1	B	1002	G	M
Specification indicating MIL-PRF-32192	Resistance ratio characteristic (see 1.2.2)	Specification sheet number indicating MIL-PRF-32192/1	Termination material (see 1.2.3)	Zero power resistance (see 1.2.4)	Zero power resistance tolerance (see 1.2.5)	Product level designator (see 1.2.6)

1.2.2 Resistance ratio characteristic. The characteristic is identified by a one-letter symbol in accordance with table I.

Comments, suggestions, or questions on this document should be addressed to DLA Land and Maritime, ATTN: VAT, Post Office Box 3990, Columbus, OH 43218-3990, or emailed to resistor@dla.mil. Since contact information can change, you may want to verify the currency of this address information using the ASSIST Online database at https://assist.dla.mil.

AMSC N/A FSC 5905

1.2.3 Termination material. The termination material designation is in accordance with table II.

1.2.4 Zero power resistance. The direct current (dc) zero power resistance measured at 25°C (see 4.8.2) and expressed in ohms is identified by a four-digit number. The first three digits represent significant figures, and the last digit specifies the number of zeros to follow. When the value of resistance is less than 100 ohms, or when fractional values of an ohm are required, the letter "R" is substituted for one of the significant digits to represent the decimal point. When the letter "R" is used, succeeding digits of the group represent significant figures. The standard resistance values for every decade follows the sequence demonstrated for the "10 to 100" decade in table III. Resistance values not listed are considered as not conforming to the specification.

TABLE I. Resistance ratio characteristic.

Symbol	Resistance ratio characteristic
A	19.8 ±10 percent
B	29.4 ±10 percent
C	48.7 ±10 percent
E	0.53 ±10 percent
D	7.1 ±10 percent
H	13.0 ±10 percent
L	16.1 ±10 percent
M	23.3 ±10 percent
N	38.5 ±10 percent
R	62.5 ±10 percent
X	142.9 ±10 percent

TABLE II. Termination materials.

Type	Material	Termination area	Code letters
Solderable	Base metallization barrier metal, solder coated	Wraparound	B
Epoxy bondable	Gold	Wraparound	G
	Platinum gold	Wraparound One surface	U T
	Palladium/silver or Platinum/silver	Wraparound	C
	Palladium/silver or Platinum/silver	One surface	D
Wire bondable	Silver	Wraparound or two surfaces	S
	Gold		W

TABLE III. Standard resistance values for the 10 to 100 decade by tolerance.

1.0%	2.0% 5.0%	10.0%	1.0%	2.0% 5.0%	10.0%	1.0%	2.0% 5.0%	10.0%	1.0%	2.0% 5.0%	10.0%
10.00	10.00	10.00	18.70	-----	-----	33.20	-----	-----	59.00	-----	-----
10.20	-----	-----	19.10	-----	-----	34.00	-----	-----	60.40	-----	-----
10.50	-----	-----	19.60	-----	-----	34.80	-----	-----	61.90	-----	-----
10.70	-----	-----	20.00	20.00	-----	35.70	-----	-----	-----	62.00	-----
11.00	11.00	-----	20.50	-----	-----	-----	36.00	-----	63.40	-----	-----
11.30	-----	-----	21.00	-----	-----	36.50	-----	-----	64.90	-----	-----
11.50	-----	-----	21.50	-----	-----	37.40	-----	-----	66.50	-----	-----
11.80	-----	-----	-----	22.00	22.00	38.30	-----	-----	-----	68.00	68.00
-----	12.00	12.00	22.10	-----	-----	-----	39.00	39.00	68.10	-----	-----
12.10	-----	-----	22.60	-----	-----	39.20	-----	-----	69.80	-----	-----
12.40	-----	-----	23.20	-----	-----	40.20	-----	-----	71.50	-----	-----
12.70	-----	-----	23.70	-----	-----	41.20	-----	-----	73.20	-----	-----
13.00	13.00	-----	-----	24.00	-----	42.20	-----	-----	75.00	75.00	-----
13.30	-----	-----	24.30	-----	-----	-----	43.00	-----	76.80	-----	-----
13.70	-----	-----	24.90	-----	-----	43.20	-----	-----	78.70	-----	-----
14.00	-----	-----	25.50	-----	-----	44.20	-----	-----	80.60	-----	-----
14.30	-----	-----	26.10	-----	-----	45.30	-----	-----	-----	82.00	82.00
14.70	-----	-----	26.70	-----	-----	46.40	-----	-----	82.50	-----	-----
15.00	15.00	15.00	-----	27.00	27.00	-----	47.00	47.00	84.50	-----	-----
15.40	-----	-----	27.40	-----	-----	47.50	-----	-----	86.60	-----	-----
15.80	-----	-----	28.00	-----	-----	48.70	-----	-----	88.70	-----	-----
16.20	-----	-----	28.70	-----	-----	49.90	-----	-----	90.90	-----	-----
16.50	-----	-----	29.40	-----	-----	-----	51.00	-----	-----	91.00	-----
16.90	-----	-----	-----	30.00	-----	51.10	-----	-----	93.10	-----	-----
17.40	-----	-----	30.10	-----	-----	52.30	-----	-----	95.30	-----	-----
17.80	-----	-----	30.90	-----	-----	53.60	-----	-----	97.60	-----	-----
-----	18.00	18.00	31.60	-----	-----	54.90	-----	-----	-----	-----	-----
18.20	-----	-----	32.40	-----	-----	-----	56.00	56.00	-----	-----	-----
-----	-----	-----	-----	33.00	33.00	56.20		-----	-----	-----	-----
-----	-----	-----	-----	-----	-----	57.60		-----	-----	-----	-----

1.2.5 Zero power resistance tolerance. The zero power resistance tolerance is identified by a single letter in accordance with table IV.

TABLE IV. Resistance tolerance versus temperature for each resistance tolerance.

Sequence	Temperature	F (±1 percent)	G (±2 percent)	J (±5 percent)	K (±10 percent)
1	-55	1/ 10 (15)	1/ 12 (17)	1/ 15 (20)	1/ 20 (25)
2	-15	1/ 5 (9)	1/ 6 (10)	1/ 9 (13)	1/ 14 (18)
3	0	3	4	7	12
4	25	1	2	5	10
5	50	3	4	7	12
6	75	5	6	9	14
7	100	7	9	12	17
8	125	10	12	15	20

1/ The percentages in parentheses are for positive coefficient thermistors.

1.2.6 Product level designator. The product level designator is identified by a single letter which denotes a military grade thermistor (M).

1.2.7 Style. The style (see 3.1) is identified by the symbol RCTP and RCTN followed by a four digit number. The letters identifies resistor, chip, thermal, positive or negative, and the four digit number identifies the physical configuration.

2. APPLICABLE DOCUMENTS

2.1 General. The documents listed in this section are specified in sections 3 and 4 of this specification. This section does not include documents cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements documents cited in sections 3 and 4 of this specification, whether or not they are listed.

2.2 Government documents.

2.2.1 Specifications, standards, or handbooks. The following specifications, standards, and handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATIONS

MIL-PRF-32192/1	-	Resistor, Chip, Thermal (Thermistor), Positive Temperature Coefficient, Style RCTP0303
MIL-PRF-32192/2	-	Resistor, Chip, Thermal (Thermistor), Insulated, Positive Temperature Coefficient, Style RCTP0805
MIL-PRF-32192/3	-	Resistor, Chip, Thermal (Thermistor), Negative Temperature Coefficient, Style RCTN0404
MIL-PRF-32192/4	-	Resistor, Chip, Thermal (Thermistor), Insulated, Negative Temperature Coefficient, Style RCTN0805
MIL-PRF-32192/5	-	Resistor, Chip, Thermal (Thermistor), Insulated, Negative Temperature Coefficient, Style RCTN1206

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-202	-	Electronics and Electrical Component Parts.
MIL-STD-202-104	-	Test Method Standard Method 104, Immersion.
MIL-STD-202-106	-	Test Method Standard Method 106, Moisture Resistance.
MIL-STD-202-107	-	Test Method Standard Method 107, Thermal Shock.
MIL-STD-202-108	-	Test Method Standard Method 108, Life (At Elevated Ambient Temperature).
MIL-STD-202-204	-	Test Method Standard Method 204, Vibration, High Frequency.
MIL-STD-202-208	-	Test Method Standard Method 208, Solderability.
MIL-STD-202-210	-	Test Method Standard Method 210, Resistance to Soldering Heat.
MIL-STD-202-213	-	Test Method Standard Method 213, Shock (Specified Pulse).
MIL-STD-202-215	-	Test Method Standard Method 215, Resistance to Solvents.
MIL-STD-790	-	Established Reliability and High Reliability Qualified Products List (QPL) Systems for Electrical, Electronic, and Fiber Optic Parts Specifications.
MIL-STD-1285	-	Marking Of Electrical and Electronic Parts.

* (Copies of these documents are available online at https://quicksearch.dla.mil/.)

2.3 Non-Government publications. The following documents form a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents are those cited in the solicitation or contract.

INTERNATIONAL ORGANIZATION for STANDARDS (ISO)

ISO 10012 - Measurement Management Systems: Requirements for Measuring Processes and Measuring Equipment

* ISO/IEC 17025 - The Competence of Testing and Calibration Laboratories, General Requirements for

* (Copies of this document are available online at https://www.iso.org/.)

IPC-ASSOCIATION CONNECTING ELECTRONICS INDUSTRIES (IPC)

IPC-CC-830B - Qualification and Performance of Electrical Insulation Compound for Printed Wiring Assemblies

* (Applications for copies are available online at https://www.ipc.org.)

2.4 Order of precedence. Unless otherwise noted herein or in the contract, in the event of a conflict between the text of this document and the references cited herein (except for related, specification sheets), the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Specification sheets. The individual item requirements shall be as specified herein and in accordance with the applicable specification sheet. In the event of any conflict between the requirements of this specification and the specification sheet, the latter shall govern (see 6.2).

3.2 Qualification. Thermistors furnished under this specification shall be products that are authorized by the qualifying activity for listing on the applicable qualified products list (QPL) before contract award. In addition, the manufacturer shall obtain certification from the qualifying activity that the product assurance requirements of 4.4 have been met and are being maintained. Authorized distributors that are approved to MIL-STD-790 distributor requirements by the QPL manufacturer are listed in the QPL.

3.3 QPL system. The manufacturer shall establish and maintain a QPL system for parts covered by this specification. Requirements for this system are specified in MIL-STD-790 and herein.

3.4 Materials. Materials shall be used which enable the thermistors to meet the performance requirements of this specification. Acceptance or approval of any constituent material shall not be construed as a guaranty of the acceptance of the finished product.

3.5 Interface and physical dimension requirements. The thermistors shall meet the interface and physical dimensions specified (see 3.1).

3.5.1 Termination. Unless otherwise specified, both terminations (areas) shall be available on one surface of the body of the thermistor chip (see 1.2.3).

3.5.2 Barrier metallization. The barrier metallization for the B termination (base metallization barrier metal, solder coated) shall be nickel or approved equivalent. The metallization shall be a minimum of 50 microinches.

3.5.3 Pure tin. The use of pure tin, as an underplate or final finish is prohibited both internally and externally. Tin content of resistor components and solder shall not exceed 97 percent, by mass. Tin shall be alloyed with a minimum of 3 percent lead, by mass (see 6.5.1).

3.6 Zero power resistance. Each thermistor shall have a zero-power resistance value within the specified tolerance of the nominal resistance value specified (see 3.1 and 4.8.2).

3.6.1 Resistance value deviations. All maximum deviations as specified in this section are to be considered absolute limits with the exception of the contact resistance adjustments.

3.7 Resistance ratio characteristic. The resistance ratio shall be as specified (see 3.1 and 4.8.3).

3.8 Solderability (applicable to termination B). When thermistors are tested as specified in 4.8.4, the immersed metallized surface shall be at least 95 percent covered with a new clean smooth coating and shall exhibit no demetallization or leaching of the terminal areas. The remaining 5 percent may contain only small pinholes or rough spots; these shall not be concentrated in one area. In case of dispute, the percentage of coverage with pinholes or rough spots shall be determined by actual measurement of these areas, as compared to the total area. For coverage calculations, defective areas on each termination shall be compared to the total area of the same termination.

3.9 Short time overload. When thermistors are tested as specified in 4.8.5, thermistors shall not arc, burn, char, or open circuit. The change in zero power resistance shall not exceed the value specified (see 3.1).

3.10 Low temperature storage. When thermistors are tested as specified in 4.8.6, there shall be no evidence of mechanical damage and the change in zero power resistance shall not exceed the value specified (see 3.1).

3.11 High temperature storage. When thermistors are tested as specified in 4.8.7, the change in zero power resistance shall not exceed the value specified (see 3.1).

3.12 Dissipation constant. When thermistors are tested as specified in 4.8.8, the dissipation constant shall be as specified (see 3.1).

3.13 Thermal time constant. When thermistors are tested as specified in 4.8.9, thermal time constant shall be as specified (see 3.1).

3.14 Mounting integrity.

3.14.1 Solder mounting integrity (applicable to termination B). When thermistors are tested as specified in 4.8.10.1, there shall be no evidence of mechanical damage.

3.14.2 Bondable mounting integrity (applicable to termination's G, U, T, C, and D). When thermistors are tested as specified in 4.8.10.2, there shall be no evidence of mechanical damage.

3.14.3 Wire bonding integrity (applicable to terminations S and W). When thermistors are tested as specified in 4.8.10.3, there shall be no evidence of mechanical damage.

3.15 Resistance to soldering heat. When thermistors are tested as specified in 4.8.11.1, thermistors shall show no evidence of mechanical damage, no demetallization or leaching; the change in zero power resistance shall not exceed the value specified (see 3.1).

3.16 Resistance to bonding exposure. When thermistors are tested as specified in 4.8.11.2, thermistors shall show no evidence of mechanical damage. The change in zero power resistance shall not exceed the value specified (see 3.1).

3.17 Resistance temperature characteristics. When thermistors are tested as specified in 4.8.12, the curve obtained for each thermistor shall conform to the curve specified (see 3.1) and fall within the tolerance limits specified in table IV (for the appropriate tolerance characteristic) at each of the temperature points indicated in table IV.

3.18 Thermal shock. When thermistors are tested as specified in 4.8.13, thermistors shall show no evidence of mechanical damage. The change in zero power resistance shall not exceed the value specified (see 3.1).

3.19 Moisture resistance. When thermistors are tested as specified in 4.8.14, thermistors shall show no signs of electrical damage, breaking, cracking, or loosening of the terminals. The change in zero power resistance shall not exceed the value specified (see 3.1).

3.20 Load life. When thermistors are tested as specified in 4.8.15, thermistors shall show no evidence of corrosion or other mechanical damage. The change in zero power resistance shall not exceed the value specified (see 3.1).

3.21 High temperature exposure. When thermistors are tested as specified in 4.8.16, the change in zero power resistance after 100 hours, and after 1,000 hours shall not exceed the value specified (see 3.1).

3.22 Vibration, high frequency. When thermistors are tested as specified in 4.8.17, thermistors shall show no evidence of mechanical damage. The change in zero power resistance shall not exceed the value specified (see 3.1).

3.23 Shock, specified pulse. When thermistors are tested as specified in 4.8.18, thermistors shall show no evidence of mechanical damage. The change in zero power resistance shall not exceed the value specified (see 3.1).

3.24 Immersion. When thermistors are tested as specified in 4.8.19, there shall be no evidence of mechanical damage. The change in zero power resistance shall not exceed the value specified (see 3.1).

3.25 Resistance to solvents. When thermistors are tested as specified in 4.8.20, there shall be no evidence of mechanical damage and the marking shall remain legible.

3.26 Marking legibility.

3.26.1 Marking legibility test (applicable to laser marked thermistors). When thermistors are tested as specified in 4.8.21, the marking shall remain legible.

3.27 Marking. A noncorrosive label containing the following information shall be applied to each unit package. PIN (see 1.2.1), "JAN" marking, date code, and source code. Date and source code shall be in accordance with MIL-STD-1285. The following is an example of the complete marking:

12345	CAGE
0312J	Date code and JAN marking
M32192A1	PIN
B1002GM	PIN

The date code shall be the date of the final assembly operation. The common manufacturing record shall include the same date code as that placed on the parts covered by the record. At the option of the manufacturer, thermistors may be marked (for example, laser or screen printed). The marking process must be approved by the qualifying activity based on testing specified herein. The marking shall remain legible after all tests.

3.27.1 Individual chip marking. Marking of individual chip thermistors is not required but is permitted. Chip thermistors may be marked using the following code systems. The marking requirement and code system used shall be specified on the order. If no code system is specified, the manufacturer may select the code. Abbreviated markings used due to limited space takes precedence over PIN format. Markings shall be the same four characters used to indicate resistance (see 1.2.4).

3.27.1.1 Option 1, four characters for 1.0 percent tolerances. The first three digits are significant figures and the last digit specifies the number of zeros to follow. When the value of resistance is less than 100 ohms, or when fractional values of an ohm are required, the letter “R” shall be substituted for one of the significant digits to represent the decimal point. When the letter “R” is used, succeeding digits of the group represent significant figures.

Example: 5.62 ohms = 5R62
14.7 ohms = 14R7
30.1 kohms = 3012

3.27.1.2 Option 2, three characters for 2, 5, and 10 percent tolerances. The first two digits are significant figures and the last digit specifies the number of zeros to follow. When the value of resistance is less than 10 ohms, or when fractional values of an ohm are required, the letter “R” shall be substituted for one of the significant digits to represent the decimal point. When the letter “R” is used, succeeding digits for the group represents significant figures.

Example: 9.7 ohms = 9R7
330 kohms = 334
12 ohms = 120

3.27.2 JAN and J marking. The United States Government has adopted, and is exercising legitimate control over the certification marks "JAN" and "J", respectively, to indicate that items so marked or identified are manufactured to, and meet all the requirements of specifications. Accordingly, items acquired to, and meeting all of the criteria specified herein and in applicable associated specifications shall bear the certification mark "JAN" except that items too small to bear the certification mark "JAN" shall bear the letter "J". The "JAN" or "J" shall be placed immediately before the part number except that if such location would place a hardship on the manufacturer in connection with such marking, the "JAN" or "J" may be located on the first line above or below the part number. Items furnished under contracts or orders which either permit or require deviation from the conditions or requirements specified herein or in applicable specifications shall not bear "JAN" or "J". In the event an item fails to meet the requirements of this specification and the applicable specification sheets, the manufacturer shall remove completely the military part number and the "JAN" or "J" from the sample tested and also from all items represented by the sample. The “JAN” or “J” certification mark shall not be used on products acquired to contractor drawings or specifications. The United States Government has obtained Certificate of Registration Number 504,860 for the certification mark "JAN" and Registration Number 2,577,735 for the certification mark “J”.

3.28 Recycled, recovered, environmentally preferable, or biobased materials. Recycled, recovered, environmentally preferable or biobased materials should be used to the maximum extent possible, provided that the material meets or exceeds the operational and maintenance requirements, and promotes economically advantageous life cycle costs.

3.29 Workmanship. Thermistors shall be processed in a manner as to be uniform in quality and shall be free from holes, fissures, chip, and malformation. The thermistors shall be free from other defects that affect life, serviceability, or appearance.

4. VERIFICATION

4.1 Classification of inspections. The inspection requirements specified herein are classified as follows:

a. Qualification inspection (see 4.4).

b. Verification of qualification (see 4.5).

c. Conformance inspection (see 4.6).

d. Periodic inspection (see 4.7)

4.2 Reliability and quality.

4.2.1 QPL system. The manufacturer shall establish and maintain a QPL system as described in 3.3. Evidence of such compliance is a prerequisite for qualification and verification of qualification.

4.3 Inspections conditions and precautions.

4.3.1 Inspection conditions. Unless otherwise specified herein, all inspections shall be performed in accordance with the test conditions specified in the general requirements of MIL-STD-202.

4.3.2 Precautions. Adequate precautions shall be taken during inspection to prevent condensation of moisture on thermistors, except during the moisture resistance temperature cycling tests.

* 4.3.3 Test equipment and inspection facilities. The manufacturer shall establish and maintain a calibration system in accordance with ISO/IEC 17025, ISO 10012, or equivalent system as approved by the qualifying activity.

4.4 Qualification inspection. Qualification inspection shall be performed at a laboratory acceptable to the Government (see 6.3) on sample units produced with and procedures normally used in production.

4.4.1 Sample. The number of sample units comprising a sample of thermistors to be submitted for qualification inspection shall be as specified in appendix A to this specification. The sample shall be taken at random from a production run and shall be produced with equipment and procedures normally used in production and which have been subjected to and passed the requirements of group A inspection (see 4.6.2). Qualification shall not be granted if group A inspection requirements are not complied with.

4.4.2 Test routine. Sample units shall be subjected to the qualification inspection specified in table V, in the order shown. All sample units with the exception of those for group II shall be subjected to the inspection of group I. The 50 sample units from group I shall than be divided as specified in table V for group III to group VII inclusive, and subjected to the inspection for their particular group.

4.4.3 Failures. Failures in excess of those allowed in table V shall be cause for refusal to grant qualification.

4.5 Verification of qualification. Every 12 months the manufacturer shall provide verification of qualification to the qualifying activity. Continuation of qualification is based on meeting the following requirements.

a. MIL-STD-790 program.

b. Design of the thermistor has not been modified.

c. Lot rejection for group A inspection does not exceed the group A sampling plan.

d. The requirements for group B inspection are met.

TABLE V. Qualification inspection.

Inspection	Requirement paragraph	Method paragraph	Number of sample units	Allowable defects 1/
Group I				
Visual and mechanical inspection 2/ 3/	3.5, 3.26, 3.27, and 3.29	4.8.1	All sample units 4/	0
Zero power resistance 3/	3.6	4.8.2		
Resistance ratio characteristic 3/	3.7	4.8.3		
Group II				
Solderability	3.8	4.8.4	12	
Resistance to solvents 5/	3.25	4.8.20	12	
Marking legibility test (laser marking)	3.26.1	4.8.21	12	
Group III				2
Short time overload	3.9	4.8.5		
Low temperature storage	3.10	4.8.6		
High temperature storage	3.11	4.8.7		
Dissipation constant 3/	3.12	4.8.8	10	
Thermal time constant 3/	3.13	4.8.9		
Solderable mounting integrity 6/	3.14.1	4.8.10.1		
Bondable mounting integrity 7/	3.14.2	4.8.10.2		
Wire bonding integrity 8/	3.14.3	4.8.10.3		
Group IV				
Resistance to soldering heat 6/	3.15	4.8.11.1		
Resistance to bonding exposure 7/	3.16	4.8.11.2		
Resistance temperature characteristic 3/	3.17	4.8.12	10	
Thermal shock	3.18	4.8.13		
Moisture resistance	3.19	4.8.14		
Group V				
Load life	3.20	4.8.15	10	2
Group VI				
High temperature exposure	3.21	4.8.16	10	
Group VII				
Vibration, high frequency	3.22	4.8.17		
Shock, specified pulse	3.23	4.8.18	10	
Immersion	3.24	4.8.19		

1/ Failure of the same thermistor in one or more tests of a group shall be charged as a single defective thermistor.
2/ Marking (where applicable) shall be considered defective only if the marking is incorrect, incomplete, or illegible.
3/ Nondestructive tests
4/ Sample units for group II shall not be subjected to group I.
5/ Test applicable for marking other than laser marked parts.
6/ Applicable to termination B.
7/ Applicable to terminations C, D, G, T, and U.
8/ Applicable to terminations S and W.

4.6 Conformance inspection.

4.6.1 Inspection of product for delivery. Inspection of product for delivery shall consist of group A and group B tests; however, group B tests shall not delay delivery.

4.6.1.1 Inspection lot. An inspection lot shall consist of all thermistors of the same style, resistance ratio, characteristic, termination type, and protective enclosure or coating under essentially the same conditions and offered for inspection during a period of 1 month.

4.6.2 Group A inspection. Group A inspection shall consist of the inspections specified in table VI, and shall be made on the set of sample units, in the order shown. Thermistors subjected to subgroup 2 shall not be supplied against purchase order.

4.6.2.1 Subgroup 1. A sample of parts from each inspection lot shall be randomly selected in accordance with table VII. If one or more defects are found, the lot shall be screened and defectives removed. After screening and removal of defectives, a new sample of parts shall be randomly selected in accordance with table VII. If one or more defects are found in this second sample, the lot shall be rejected and shall not be supplied to this specification.

4.6.2.2 Subgroup 2 (solderability). A sample of parts from each inspection lot shall be selected randomly in accordance with table VII and subjected to the subgroup 2 solderability test. The manufacturer may use electrical rejects from subgroup 1 screening tests for all or part of the samples to be used for solderability testing. If there are one or more defects, the lot shall be considered to have failed.

4.6.2.2.1 Rejected lots. In the event of one or more defects, the inspection lot is rejected. If the lot fails this solderability test, the lot may be reworked and retested. Any inspection lot that fails the solderability retest shall be considered to have failed and that lot shall not be supplied to the requirements of the specification.

TABLE VI. Group A Inspection.

Inspection	Requirement paragraph	Method paragraph	Sampling procedure
Subgroup 1			
Visual and mechanical examination			
Thermistor body dimensions	3.5		
Marking 1/	3.27	4.8.1	
Workmanship	3.29		4.6.2.1
Zero power resistance	3.6	4.8.2	
Resistance ratio characteristic	3.7	4.8.3	
Subgroup 2 2/			
Solderability	3.8	4.8.4	4.6.2.2

1/ Marking defects shall be charged only for illegible or incomplete marking. Any subsequent electrical defect shall not be charged as a marking defect.

2/ The manufacturer may request the deletion of the subgroup 2 solderability test, providing an in line process control system for assessing the solderability of terminations can be validated and approved by the qualifying activity. Deletion of the test does not relieve the manufacturer from meeting this test requirement in case of dispute. If the design, material, construction, or processing of the part is changed or if there are any problems, the qualifying activity may require resumption of the test.

TABLE VII. Group A sampling plan.

Lot size	Subgroup 1 sample size	Subgroup 2 sample size
1 to 125	100 percent	5
126 to 3,200	125	5
3,201 to 10,000	125	8
10,001 to 35,000	294	13
35,001 to 150,000	294	20
150,001 to 500,000	345	20
500,001 and over	435	20

4.6.2.2.2 Disposition of samples. The solderability test is considered a destructive test and samples submitted to the solderability test shall not be supplied on the contract.

4.6.3 Group B inspection. Group B inspection shall consist of the test specified in table VIII in the order shown. Unless the Government considers it more practical to select a separate sample from the lot for group B inspection, they shall be performed on sample units that have passed the group A tests.

TABLE VIII. Group B inspection.

Inspection	Requirement paragraph	Method paragraph	Sampling procedure
Subgroup 1 1/			
Short time overload	3.9	4.8.5	See 4.6.3.1
Low temperature storage	3.10	4.8.6	
High temperature storage	3.11	4.8.7	
Subgroup 2 1/			
Resistance to solvents 2/	3.25	4.8.20	See 4.6.3.2
Subgroup 3			
Solder mounting integrity 3/	3.14.1	4.8.10.1	See 4.6.3.3
Bondable mounting integrity 4/	3.14.2	4.8.10.2	
Wire bonding integrity 5/	3.14.3	4.8.10.3	

1/ If the manufacturer can demonstrate that this test has been performed five consecutive times with zero failures, the frequency of this test, with the approval of the qualifying activity, can be performed on an annual basis. If the design, material, constructions, or processing of the part is changed, or if there are any quality problems or failures, the qualifying activity may require resumption of the original test frequency.
2/ Test applicable for marking other than laser marked parts.
3/ Applicable to termination B.
4/ Applicable to terminations G, U, T, C, and D.
5/ Applicable to terminations S and W.

4.6.3.1 Subgroup 1. A sample of parts shall be randomly selected in accordance with table IX. If one or more defects are found, the lot shall be screened and defectives removed. After screening and removal of defectives, a new sample of parts shall be randomly selected in accordance with table IX. If one or more defects are found in the second sample, the lot shall be rejected and shall not be supplied to this specification.

TABLE IX. Group B sampling plan.

Lot size	Sample size
1 to 25	3
26 to 50	5
51 to 90	6
91 to 150	7
151 to 280	10
281 to 500	11
501 to 1,200	15
1,201 to 3,200	18
3,201 to 10,000	22
10,001 and over	29

4.6.3.2 Subgroup 2. Twelve samples shall be selected randomly from each inspection lot. If one or more defects are found, the lot shall be screened and defectives removed. After screening and removal of defectives, a new sample of twelve parts shall be randomly selected. If one or more defects are found in the second sample, the lot shall be rejected and shall not be supplied to this specification.

4.6.3.3 Subgroup 3. Twelve samples shall be selected randomly from each inspection lot. If one or more defects are found, the lot shall be screened and defectives removed. After screening and removal of defectives, a new sample of twelve parts shall be randomly selected. If one or more defects are found in the second sample, the lot shall be rejected and shall not be supplied to this specification.

4.6.3.4 Disposition of sample units. Sample units that have passed group B inspection shall not be delivered on the contract or purchase order.

4.7 Periodic inspection. Periodic inspection shall consist of group C inspection. Except where the results of these inspections show noncompliance with the applicable requirements (see 4.7.4), delivery of products which have passed group A and group B inspections shall not be delayed pending the results of these periodic inspections.

4.7.1 Group C inspection. Group C inspection shall consist of the tests specified in table X, in the order shown. They shall be performed on sample units of each style and characteristic selected from lots that have passed group A and group B inspections. The sample units used in group B inspection are not to be used in group C inspection.

TABLE X. Group C inspection.

Inspection	Requirement paragraph	Method paragraph	Number of sample units to be tested
Monthly 1/			
Dissipation constant	3.12	4.8.8	
Thermal time constant	3.13	4.8.9	10
Quarterly - Subgroup 1 1/			
Resistance temperature characteristic	3.17	4.8.12	
Thermal shock	3.18	4.8.13	
Resistance to soldering heat	3.15	4.8.11.1	
Resistance to bonding exposure	3.16	4.8.11.2	10
Moisture resistance	3.19	4.8.14	
Quarterly - Subgroup 2			
Load life	3.20	4.8.15	10
Quarterly - Subgroup 3 1/			
High temperature exposure	3.21	4.8.16	10
Semiannually 2/			
Vibration, high frequency	3.22	4.8.17	
Shock, specified pulse	3.23	4.8.18	10
Immersion	3.24	4.8.19	

1/ If the manufacturer can demonstrate that these tests have been performed for five consecutive times with zero failures, these tests, with the approval of the qualifying activity, can be deleted. The manufacturer however, shall perform these tests every three years after the deletion as part of long term design verification. If the design, material, construction, or processing of the part is changed, or if there are any problems, the qualifying activity may require resumption of the specified testing. Deletion of testing does not relieve the manufacturer from meeting the test requirement in case of dispute.

2/ If the manufacturer can demonstrate that these tests have been performed for five consecutive times with zero failures, these tests, with the approval of the qualifying activity, can be deleted. The manufacturer however, shall perform these tests every five years after the deletion as part of long term design verification. If the design, material, construction, or processing of the part is changed, or if there are any problems, the qualifying activity may require resumption of the specified testing. Deletion of testing does not relieve the manufacturer from meeting the test requirement in case of dispute.

4.7.2 Sampling plan.

4.7.2.1 Monthly. Ten sample units of any resistance value shall be inspected monthly with one defective unit allowed. If more than one sample fails the monthly tests, double the quantity of samples required shall be inspected with no defective units allowed.

4.7.2.2 Quarterly. Thirty sample units of any zero power resistance between the middle value and the highest value for which qualification is sought shall be inspected quarterly. Ten sample units shall be subjected to the tests of group 1, and ten sample units of the value closest to the value above the middle value shall be subjected to the tests of subgroup 2. In addition, ten sample units shall be subjected to the tests of subgroup 3. One defective unit shall be allowed for each subgroup, but not more than one defective for the three groups combined.

4.7.2.3 Semiannually. Ten sample units of the highest resistance value shall be inspected semiannually, with one defective unit allowed.

4.7.3 Disposition of sample units. Sample units which have been subjected to group C inspection shall not be delivered on the contract or purchase order.

4.7.4 Noncompliance. If a sample fails to pass group C inspection, the supplier shall take corrective action on the materials or processes, or both, as warranted, and on all units of product which can be corrected and which were manufactured under essentially the same conditions, with essentially the same materials, and processes, and which are considered subject to the same failure. Acceptance of the product shall be discontinued until corrective action, acceptable to the Government, has been taken. After the corrective action has been taken, group C inspection shall be repeated on additional sample units (all inspections, or the inspection the original sample failed, at the option of the Government). Group A and group B inspection may be reinstituted; however, final acceptance shall be withheld until group C reinspection has shown corrective action was successful. In the event of failure after reinspection, information concerning the failure and the corrective action taken shall be furnished to the contracting officer.

4.8 Methods of inspections.

4.8.1 Visual and mechanical inspection and chip mounting.

4.8.1.1 Visual and mechanical inspection. Unless otherwise specified, thermistors shall be examined under 30X magnification to verify that the materials, design, construction, physical dimensions, and workmanship are in accordance with the applicable requirements. A protective coating (where applicable) is applied over the thermistor element for mechanical and environmental protection. Reject for coating damage which exposes the underlying thermistor element and any visible cracks in the coating. (see 3.1, 3.5, 3.26, 3.27, and 3.29).

4.8.1.2 Chip mounting procedures. When specified herein, the chip thermistor shall be mounted on a test board as described in 4.8.1.3. For those test procedures where mounting requirements are unspecified, the chip thermistors shall be tested unmounted using pressure contacts. Pressure contacts shall not cover more than 10 percent of the termination area.

4.8.1.3 Specified mounting. When specified in the test procedure, the chip thermistor shall be mounted on a test board as specified on figure 1. The test board material shall be such that it shall not be the cause of, nor contribute to, any failure of a chip thermistor in any of the tests for which it may be used. The test board shall be prepared with metallized surface land areas of proper spacing so that a test board surface area of at least four times the thermistor chip surface area is provided for each thermistor chip mounted. The metallized surface land areas shall be designed in a pattern to accommodate a number of thermistor chips. The metallization material shall be compatible with the bonding technique to be employed and the material used on the chip termination. The method of chip mounting for the different termination materials shall be as follows:

a. Termination B (solderable). Termination B chip thermistors shall be mounted on a fiberglass test board by soldering the chip terminations directly to the test board metallized land areas in the following manner:

    (1) Solder and soldering flux shall be of such a quality as to enable the chip thermistors to meet all the requirements of this specification and shall be applied to the terminations of each chip of code letter B (see 1.2.3).

    (2) All chips shall be placed across the metallized land areas of the test board with contact between the chip termination's and board land areas only. The use of adhesive to keep chips in place during mounting operation is allowable except for preparation of solder mounting integrity test pieces.

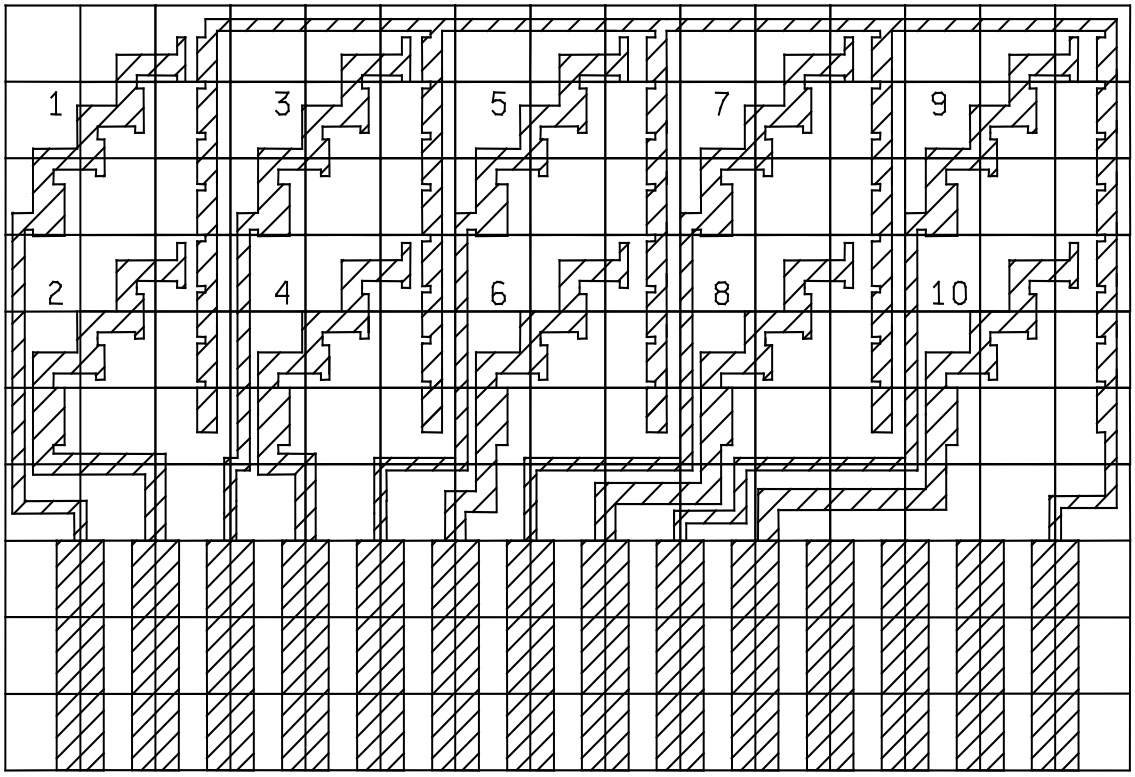
    (3) For resistance to soldering heat, the test board with all chips in position shall be placed on a heat transfer unit (molten solder, hot plate, or tunnel oven) with the temperature transitioned to 245°C ±5°C. The chips shall remain at 245°C ±5°C until the solder melts and reflows forming a homogenous solder bond.

    (4) For load life, the test board with all chips in position shall be placed on a heat transfer unit (molten solder, hot plate, or tunnel oven) with a time and temperature to assure proper reflow mounting.

b. Terminations G, U, T, C, and D (epoxy bondable). As an alternative to 4.8.1.3.a(1), chip thermistors may be mechanically attached to the ceramic test board with type 2 epoxy approved by the qualifying activity. The epoxy shall be cured at a minimum temperature of 150°C. The minimum curing time shall be 30 minutes.

c. Terminations S and W (wire bondable). Chip thermistors with wire bondable termination's shall be mechanically attached to the test board and electrically connected by wire bonding flying lead interconnections between the chip termination and the ceramic test board metallized land areas. The interconnecting lead shall be .001 inch (0.03 mm) in diameter gold wire. The chip shall be mechanically or adhesively mounted by any procedure which shall not be the cause of or contribute to any failures of the chip thermistor in any test.

4.8.1.3.1 Fiberglass base board. Fiberglass base boards can be FR-4, G-10, G-30, or equivalent. When specified, a fiberglass test board with copper lamination shall be used for testing. The copper lamination shall be 70 micrometers copper (2 ounces) thickness (maximum).



NOTES:

1. Suggested ceramic test board (e.g., 96 percent alumina): 1.000 inch (25.40 mm) x 1.500 inch (38.10 mm) x 0.025 inch (0.64 mm) thick.
* 2. Suggested fiberglass test board (e.g., G30 or FR-4 glass epoxy): 1.000 inch (25.40 mm) x 1.500 inch (38.10 mm) x 0.0625 inch thick (1.5875 mm).
* 3. The contacts fit a printed circuit board connector with 0.100 inch (2.54 mm) in contact center.
4. Short lead wire may be soldered on and it shall then fit a microcircuit connector, or test lead wires may soldered on for direct measurement.
5. Small grid square are 0.100 inch (0.25 mm).
6. A larger test board, to suitable scale, may be used to accommodate additional test samples or additional style/size configurations.

FIGURE 1. Suggested test board.

4.8.2 Zero power resistance (see 3.6 and 6.8.3).

4.8.2.1 Measurements. All resistance measurements shall be made in a controlled uniform medium capable of maintaining an accuracy in temperature of ±0.05°C.

4.8.2.2 Equipment sensitivity.

a. Resistance: A Wheatstone bridge, or equivalent, accuracy to ±0.05 percent or better.

b. Temperature: The time response of the temperature indicator shall be compatible with that of the thermistor being tested.

4.8.2.3 Test procedure. The test procedure shall be as follows:

a. Temperature stabilization: Allow enough time for medium and thermistor to stabilize at required temperatures.

b. Measurements: Measure zero power resistance at 25°C and 125°C. With the input voltage disconnected, adjust the output indicator to the zero output position. Connect input voltage source and measure zero power resistance. Disconnect the voltage source. If the output does not return to its initial zero output position to within a tolerance equivalent to ±0.05 percent of the resistance value, the thermistor shall be classified as defective.

4.8.3 Resistance ratio characteristic (see 3.7 and 6.8.4). Compute the resistance ratio using the zero power resistance measurement at 25°C and 125°C (see 4.8.2).

4.8.4 Solderability (applicable to termination B) (see 3.8). Thermistors shall be tested in accordance with MIL-STD-202-208. Both end terminations shall be immersed completely one at a time or both at the same time by dipping the entire chip in the solder pot. The following details and exceptions shall apply:

a. Apparatus:

(1) A solder pot capable of keeping the solder temperature to ±5°C of setpoint.

(2) A device to keep the specimen submerged in solder for the required time.

(3) Optical equipment capable of 30X magnification.

(4) A laboratory beaker or appropriate laboratory apparatus that is capable of:

(a) Supporting a nonmetallic device.

(b) Maintaining the test specimens at a distance of 1.50 inches (38.1 mm) to 2.50 inches (63.5 mm) from the surface of the boiling deionized water (DI) or distilled water while, at the same time, exposing them to the full flow of steam generated.

b. The requirement for standard solderable wire application shall not apply.

c. The immersion and emersion rates shall not apply.

d. The specimen shall be totally submerged for at least 5 seconds.

4.8.5 Short time overload (see 3.9).

4.8.5.1 Test procedures. The test procedure shall be as follows:

a. Obtain zero power resistance at 25°C.

b. Provide a filtered regulated dc power supply or battery.

c. Ambient: Room temperature.

d. Using the value of dissipation constant and nominal resistance value specified (see 3.1), compute the average value of E_{th} and I_{th} required to raise the thermistor to the maximum power rating. Place the unit in a circuit accomplishing this.

e. Energize the circuit for 5 minutes.

f. De-energize the circuit for 10 minutes. Repeat this operation for ten complete cycles.

g. Examine thermistor for evidence of arcing, burning, or charring.

h. Sixty minutes removal from circuit, the zero power resistance shall again be measured as specified in 4.8.2 (see 3.6).

4.8.6 Low temperature storage (see 3.10). Zero power resistance shall be measured at 25°C as specified in 4.8.2. Within 1 hour after this measurement, the thermistors shall be placed in a cold chamber at room temperature. The temperature shall be reduced to -62°C ±3°C, and the thermistor maintained at that temperature for a period of not less than 3 hours. Thermistors shall be isolated from metal surface of cold boxes. (For conformance inspection only, at option of the supplier, the thermistor may be placed in the cold chamber when it is already at the extreme low temperature.) The thermistors shall then be removed from the chamber and stabilized at room temperature. The final zero power resistance at 25°C shall be measured as specified in 4.8.2, not less than 1 hour from termination of the test and within a 24 hour period. The thermistors shall then be examined for mechanical damage.

4.8.7 High temperature storage (see 3.11). Measure the zero power resistance of all test samples. Thermistors shall be isolated from metal surfaces of ovens.

a. Temperature: The temperature shall be within ±2 percent (in °C) of the maximum operating temperature specified (see 3.1).

b. Load condition: No load.

c. Duration: Test duration shall be 100 hours.

d. Resistance measurement: Measure and record zero power resistance 1 hour to 24 hours later in an ambient temperature 25°C.

4.8.8 Dissipation constant (see 3.12 and 6.8.8). The test procedure shall be as follows:

a. Measure zero power resistance at 25°C and 75°C (see 4.8.2).

b. Power supply: Use a dc regulated or battery power supply.

c. Place thermistors in a still air controlled chamber with a minimum volume of 1,000 times the thermistor body and test fixture. Chamber temperature shall be 25°C ±1°C.

d. Loading (see figure 2): Adjust E_{th} and I_{th} for zero power resistance values of 75°C. Keep load for maximum of 15 minutes.

e. Voltage and current measurements shall be performed with a high impedance measuring circuit of an accuracy ±1 percent or better.

f. Record I_{th} and E_{th}.

g. Compute and record the dissipation constant:

$$\frac{P}{50} = \frac{E_{th} \times I_{th}}{75°C - 25°C} \quad \text{(milliwatts/°C)}$$

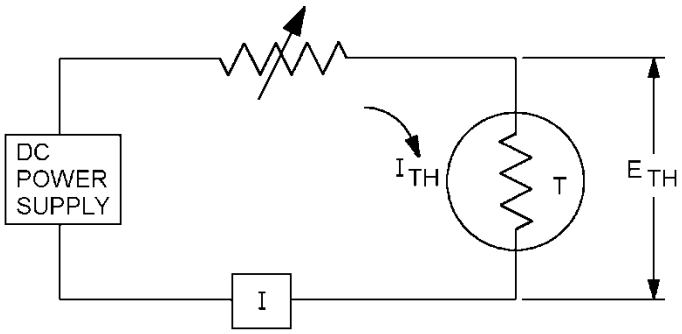


FIGURE 2. Measuring circuit.

4.8.9 Thermal time constant (see 3.13, 6.8.9, and figure 3). The test procedure shall be as follows:

a. Measure and record zero power resistance at 43.4°C and 75°C (see 4.8.2).

b. Power supply: Use a dc regulated power supply or battery.

c. Place thermistors in a still air controlled chamber with a minimum volume of 1,000 times the thermistor body and test fixture.

d. With switch AA closed, adjust E_{th}/I_{th} ratio equal to the zero power resistance at 75°C. Allow 15 minutes (maximum) for stabilization of thermistors.

e. Set bridge (see figure 3) for null with the zero power resistance value measured at 43.4°C in 4.8.9.a.

f. Prepare to measure time from the instant the switch is thrown to position BB to the time the bridge indicator passes through the null point. Throw switch to BB position and record time.

g. Chamber temperature: 25°C ±1°C.

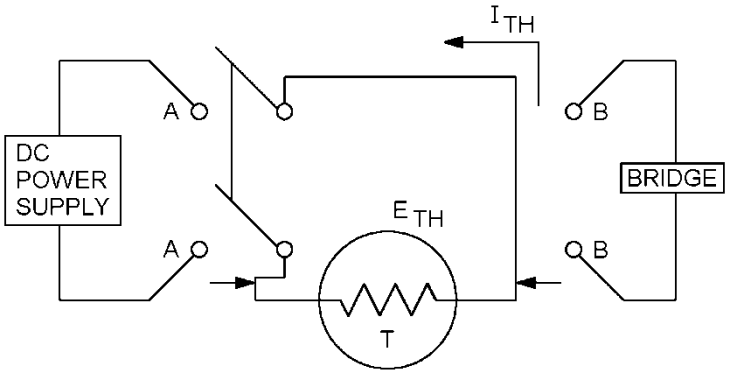


FIGURE 3. Test circuits for time constant of thermistors.

4.8.10 Mounting integrity.

4.8.10.1 Solder mounting integrity (termination B (see 3.14.1)). The thermistor chips shall be prepared as specified in 4.8.1.3a. A force shall be applied to all solderable units. The force shall be applied to the edge of the chip as shown on figure 4 for a minimum of 30 seconds. The thermistor shall be examined for evidence of mechanical damage. The pusher width shall be a minimum of 30 percent of the length and the maximum width shall be 70 percent of the chip length. The applied force shall be as specified in table XI.

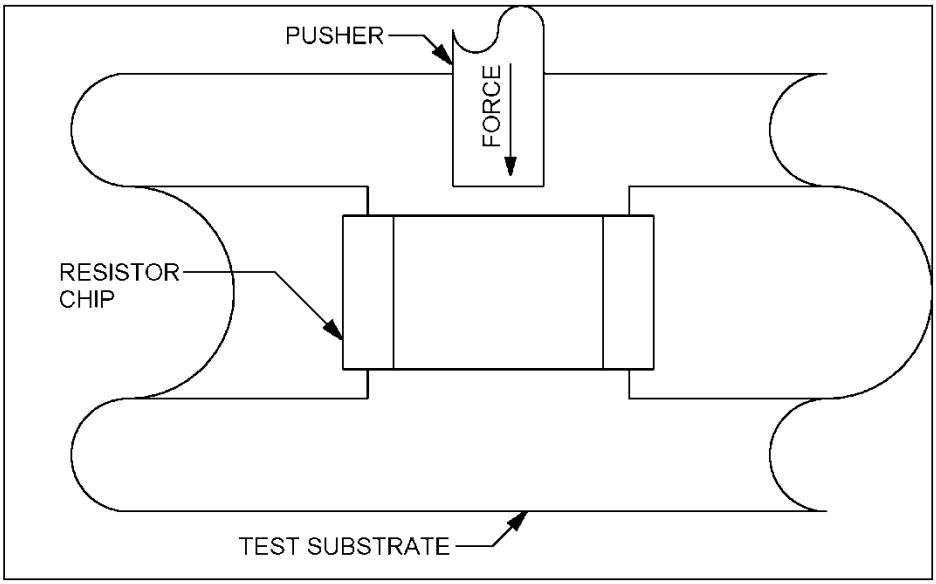


FIGURE 4. Mounting integrity test fixture.

TABLE XI. Solder mounting integrity.

Style	Force applied (kilograms)
RCTP0303, RCTN0404	0.75
RCTP0805, RCTN0805, and RCTN1206	2

4.8.10.2 Bondable mounting integrity (termination's G, U, T, C, and D (see 3.14.2)). The thermistor chips shall be prepared as specified in 4.8.1.3b. A force shall be applied to all bondable units. The force shall be applied to the edge of the chip as shown on figure 4 for a minimum of 30 seconds. The thermistor shall be examined for evidence of mechanical damage. The pusher width shall be a minimum of 30 percent of the thermistor length and the maximum width shall be 70 percent of the chip length. The applied force shall be as specified in table XII.

TABLE XII. Bondable mounting integrity.

Style	Force applied (kilograms)
RCTP0303, RCTN0404	0.4
RCTP0805, RCTN0805, and RCTN1206	1.0

4.8.10.3 Wire bonding integrity (applicable to terminations S and W) (see 3.14.3). The chip thermistor shall be prepared as specified in 4.8.1.3c. A pull of 4 grams shall be applied by inserting a hook under the lead wire at approximately the center of the wire as shown in figure 5. The force shall be applied at a 90 degree angle to the surface of the chip, one lead at a time for a minimum of 30 seconds each.

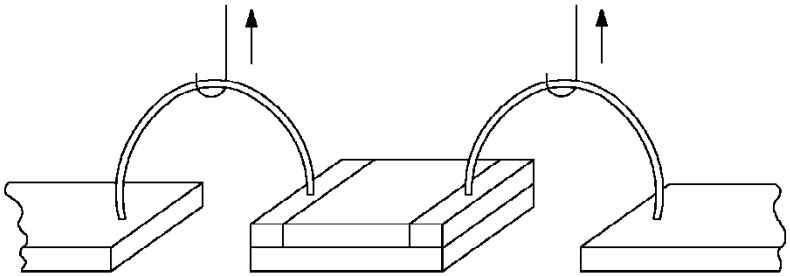


FIGURE 5. Weldable style units.

4.8.11 Resistance to soldering heat and resistance to bonding exposure.

4.8.11.1 Resistance to soldering heat (termination B) (see 3.15). Thermistors shall be tested in accordance with MIL-STD-202-210. The following details and exceptions shall apply:

a. Measurement before test: Zero power resistance shall be measured as specified in 4.8.2.

b. Mounting: Thermistors shall be mounted on a fiberglass test board as specified in 4.8.1.3.a(3). This mounting procedure shall be considered one heat cycle.

c. Second heat cycle: Test condition J, except this is the last heat cycle. (NOTE: When a hot plate is used, the temperature shall be 245°C ±5°C for 60 seconds ±5 seconds and the temperature ramp and emersion/immersion rate does not apply.

d. Measurement after test: After completion of the cleaning process and following a stabilization period at room temperature, the zero power resistance shall be measured as specified in 4.8.2.

e. Examination after test: Thermistors shall be examined for evidence of mechanical damage.

4.8.11.2 Resistance to bonding exposure (terminations S, W, G, U, T, C, and D) (see 3.16). The zero power resistance of the chip thermistor shall be measured as specified in 4.8.2. The chip thermistor shall be mounted on a ceramic test board in accordance with 4.8.1.3. The test board, with thermistors mounted, shall be stabilized at room temperature after which the zero power resistance shall again be measured as specified in 4.8.2. Thermistors shall be examined for evidence of mechanical damage.

4.8.12 Resistance temperature characteristic (see 3.17). The thermistors shall be stabilized at each of the ambient temperatures listed in table IV. Zero power resistance measurements shall be made in accordance with 4.8.2 at each specified temperature, after a stabilization time equal to or not less than ten times the applicable thermal time constant (see 3.1). Zero power resistance shall be tabulated for each measurement.

4.8.13 Thermal shock (see 3.18). Thermistors shall be tested in accordance with MIL-STD-202-107. The following details and exceptions shall apply:

a. Measurement before cycling: Zero power resistance shall be measured at 25°C as specified in 4.8.2.

b. Test condition letter: B: For thermistors rated at 125°C, C: For thermistors rated at 200°C and at 275°C.

c. Climate chamber: The rate of temperature change within the climate chamber shall not be less than 2°C per minute. The temperature shall be maintained at each of the extreme temperatures by means of circulating air. The air temperature shall be measured by a suitable method and as near the center of the group of thermistors as possible.

d. When two climate chambers are used: The thermistors may be transferred from one chamber to another, in which case, they shall be kept at room temperature for not less than 10 minutes and not more than 15 minutes between exposure, to the extreme temperatures.

e. Measurement after cycling: Not less than 1 hour, but within a 24 hour period after the last cycle, zero power resistance shall be measured outside the chamber as specified in 4.8.2.

f. Inspection after the test: Thermistors shall be inspected for evidence of mechanical damage.

4.8.14 Moisture resistance (see 3.19). Thermistors shall be tested in accordance with MIL-STD-202-106 The following exceptions shall apply:

a. Initial measurements: Not less than one- and one-half hours after thermistors have been removed from the drying oven, the zero power resistance shall be measured at 25°C as specified in 4.8.2.

b. Loading: During the first two hours of step 2 and MIL-STD-202-106, a test potential which maintain the thermistors at their maximum power specified (see 3.1), shall be applied to 50 percent of the thermistors. The remaining 50 percent of the thermistors shall be tested without any application of voltage.

c. Final measurements: Upon completion of MIL-STD-202-106 of the final cycle, the thermistors shall be held at the high humidity state conditions and a temperature of 25°C ±2°C for a period of one and one-half hours to three and one-half hours. Zero power resistance tests shall be performed as specified in 4.8.2 within 24 hours. The sample units shall not be subjected to forced circulating air during tests.

4.8.15 Load life (see 3.20). Thermistors shall be tested in accordance with MIL-STD-202-108. The following details and exceptions shall apply:

a. Method of mounting: Unmounted (see 4.8.1.2) and the thermistor location shall be arranged so that the temperature of any one thermistor shall not appreciably influence the temperature of any other thermistor. There shall be no circulation of air over the thermistors other than that caused by the heat of the thermistors.

b. Ambient test temperature and tolerance: 25°C +5°C, -0°C.

c. Initial measurement: Zero power resistance shall be measured at a temperature of 25°C in accordance with 4.8.2.

d. Test circuit: See figure 2.

e. Operating conditions: Apply the maximum power specified (see 3.1) intermittently, one and one-half hours “on” and one-half hour “off” for 1,000 hours.

f. Test condition letter: D.

g. Measurements during test: The zero power resistance shall be measured as specified in 4.8.2, at the end of each of the one half hour “off” periods, after 250 hours ±12 hours, 500 hours ±12 hours, 750 hours ±12 hours, and 1,000 hours ±12 hours have elapsed.

h. Inspection after test: Thermistors shall be inspected for evidence of mechanical damage.

4.8.16 High temperature exposure (see 3.21). Thermistors shall be maintained at the applicable maximum temperature (see 3.1) for 1,000 hours +20 hours, -0 hours. Zero power resistance shall be measured at 25°C after 100 hours +10 hours, -0 hours, and at the end of the test. These measurements shall be taken after stabilization at 25°C not to exceed 72 hours.

4.8.17 Vibration, high frequency (see 3.22). Thermistors shall be tested in accordance with MIL-STD-202-204. The following details and exceptions shall apply:

a. Mounting: As specified in 4.8.1.3.

b. Initial measurement: Zero power resistance shall be measured at 25°C as specified in 4.8.2.

c. Test condition letter: D.

d. Direction of motion: In each of two mutually perpendicular directions, one perpendicular and the other parallel to the longitudinal axis of the thermistor.

e. Measurement during test: Each thermistor shall be monitored to determine electrical discontinuity by a method which shall be sensitive enough to monitor or register (automatically) any electrical discontinuity of 0.1 millisecond or greater duration.

f. Measurement after vibration: Zero power resistance shall be measured at 25°C as specified in 4.8.2.

g. Inspection after test: Thermistors shall be inspected for evidence of mechanical and electrical damage.

4.8.18 Shock, specified pulse (see 3.23). Thermistors shall be tested in accordance with MIL-STD-202-213. The following details and exceptions shall apply:

a. Mounting: As specified in 4.8.1.3.

b. Test condition letter: A.

c. Measurements before shock: Zero power resistance shall be measured at 25°C as specified in 4.8.2.

d. Number and direction of applied shocks: The thermistors shall be subjected to a total of ten shocks in each of two mutually perpendicular planes (one perpendicular and the other parallel to longitudinal axis of the thermistor).

e. Measurements during shock: Each thermistor shall be monitored to determine electrical discontinuity by a method which shall at least be sensitive enough to monitor or register automatically any electrical discontinuity of 0.1 millisecond or greater duration.

f. Measurement after shock: Zero power resistance shall be measured at 25°C as specified in 4.8.2.

g. Inspection after test: Thermistors shall be inspected for evidence of mechanical and electrical damage.

4.8.19 Immersion (see 3.24). Thermistors shall be tested in accordance with MIL-STD-202-104. The following details and exceptions shall apply:

a. Test condition letter: B.

b. Inspection after last cycle: There shall be no evidence of mechanical damage.

c. Resistance measurement: Measure zero power resistance not later than 24 hours after the last cycle as specified in 4.8.2.

4.8.20 Resistance to solvents (see 3.25). Thermistors shall be tested in accordance with MIL-STD-202-215. The following details shall apply:

a. Marked portion of thermistor shall be brushed.

b. The number of sample units shall be as specified in table V and table VIII, as applicable.

c. Thermistors shall be inspected for mechanical damage and legibility of markings.

4.8.21 Laser marking legibility test (see 3.26.1). Thermistors shall be coated with .005 inch (0.13 mm) minimum of silicon resin insulated compound, type SR of IPC-CC-830B or approved equivalent. After curing, coated thermistors shall be examined for legibility under normal production room lighting by an inspector at 10X magnification.

5. PACKAGING

5.1 Packaging. For acquisition purposes, the packaging requirements shall be as specified in the contract or order (see 6.2). When packaging of materiel is to be performed by DoD or in-house contractor personnel, these personnel need to contact the responsible packaging activity to ascertain packaging requirements. Packaging requirements are maintained by the Inventory Control Point's packaging activity within the Military Service or Defense Agency, or within the military services system commands. Packaging data retrieval is available from the managing Military Department's or Defense Agency's automated packaging files, CD-ROM products, or by contacting the responsible packaging activity.

6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory.)

6.1 Intended use. Thermistors covered by this specification are intended for use in electronic equipment, and are used for stringent environmental and electrical requirements. Thermistors covered by this specification are unique due to the fact that these devices must be able to operate satisfactorily in military systems under the following demanding conditions: 20 Gs of high frequency vibration, 100 Gs of shock (specified pulse), and undergo moisture resistance test. In addition these military requirements are verified under a qualification system. Commercial components are not designed to withstand these military environmental conditions.

6.2 Acquisition requirements. Acquisition documents must specify the following:

a. Title, number, and date of this date of this specification, the applicable associated specification, and the complete PIN (see 1.2.1).

b. Unless otherwise specified (see 2.1), the versions of the individual documents referenced will be those in effect on the date of release of the solicitation.

c. Packaging requirements (see 5.1).

6.3 Qualification. With respect to products requiring qualification, awards will be made only for products which are, at the time of award or contact, qualified for inclusion in Qualified Products List QPL-32192 whether or not such products have actually been so listed by that date. The attention of the contractors is called to these requirements, and manufacturers are urged to arrange to have the products that they propose to offer to the Federal Government tested for qualification in order that they may be eligible to be awarded contracts or orders for the products covered by this specification. The activity responsible for the QPL and information pertaining to qualification of products may be obtained from DLA Land and Maritime, ATTN: VQP, Post Office Box 3990, Columbus, OH 43218-3990 or by email to vqp.chief@dla.mil. An online listing of products qualified to this specification may be found in the Qualified Products Database (QPD) at https://assist.dla.mil.

6.4 Critical voltage (applicable to NTC thermistors). The current voltage characteristic curve of NTC thermistors indicates that the voltage increases with increase in current normally up to a critical voltage point. Heat produced by the current at this point causes the resistance of the thermistor to decrease, thereby resulting in a voltage drop as the current increases further. A limiting series resistor (approximately 0.100 of nominal resistance value of thermistor) is used in circuits where the maximum operating temperature might be exceeded.

6.5 Materials. There are many material grades used for construction of negative temperature coefficient thermistors, for example:

a. Composed of manganese and nickel oxides.

b. Composed of manganese, nickel, and cobalt oxides.

The conductivity of each grade is characteristic of the chemical proportion of each element, and of temperature. Other semiconductor materials such as silicon or boron are used for positive temperature coefficient thermistors. The intent of this specification is not to limit the types of materials used in the construction of thermistors. However, the units must comply with the performance requirements specified.

6.5.1 Tin whisker growth. The use of alloys with tin content greater than 97 percent, by mass, may exhibit tin whisker growth problems after manufacture. Tin whiskers may occur anytime from a day to years after manufacture and can develop under typical operating conditions, on products that use such materials. Conformal coatings applied over top of a whisker-prone surface will not prevent the formation of tin whiskers. Alloys of 3 percent lead, by mass, have shown to inhibit the growth of tin whiskers. For additional information on this matter refer to ASTM-B545 (Standard Specification for Electrodeposited Coatings of Tin).

6.6 Flammability. It should be noted that this specification contains no requirements concerning the flammability of the material used in construction of the thermistors. Users should take this into consideration when a particular application involves this requirement.

6.7 Mounting for shock and vibration. Where thermistor bodies are restrained from movement under conditions of shock and vibration, consideration must be given to the restraining techniques effect upon the thermal characteristics of the thermistor.

6.8 Definitions.

6.8.1 Thermistor. A thermistor is a thermally sensitive resistor whose primary function is to exhibit a change in electrical resistance with a change in thermistor body temperature.

6.8.2 Standard reference temperature. The standard reference temperature is the thermistor body temperature at which nominal zero power resistance is specified (25°C).

* 6.8.3 Zero power resistance (R_T). The zero power resistance is the dc resistance value of a thermistor measured at a specified temperature with a power dissipation by the thermistor low enough that any further decrease in power will result in not more than 0.1 percent (or 0.100 inch (2.54 mm) of the specified measurement tolerance, whichever is smaller) change in zero power resistance.

6.8.4 Resistance ratio characteristic. The resistance ratio characteristic identifies the ratio of the zero power resistance of a thermistor measured at 25°C to that resistance measured at 125°C (see 4.8.3).

6.8.5 Zero power temperature coefficient of resistance (alpha a_T). The zero power temperature coefficient of resistance is the ratio at a specified temperature (T), of the rate of change of zero power resistance with temperature to the zero power resistance of the thermistor.

$$a_T = \frac{1}{R_T} \frac{(d^R T)}{(dT)}$$

6.8.5.1 Negative temperature coefficient (NTC). An NTC thermistor is one which the zero power resistance decreases with an increase in temperature.

6.8.5.2 Positive temperature coefficient (PTC). An PTC thermistor is one which the zero power resistance increases with an increase in temperature.

6.8.6 Maximum operating temperature. The maximum operating temperature is the maximum thermistor body temperature at which the thermistor will operate for an extended period of time with acceptable stability of its characteristics. This temperature is the result of the internal, or external heating or both, and should not exceed the maximum value specified (see 3.1).

6.8.7 Maximum power rating. The maximum power rating of a thermistor is the maximum power which a thermistor will dissipate for an extended period of time with acceptable stability of its characteristics (see 3.1).

6.8.8 Dissipation constant. The dissipation constant is the ratio, (in milliwatts per degree C) at a specified ambient temperature, of a change in power dissipation in a thermistor to the resultant thermistor body temperature change.

6.8.9 Thermal time constant. The thermal time constant is the time required for a thermistor to change to 63.2 percent of the total difference between its initial and final thermistor body temperature when subjected to a step function change in temperature under zero power conditions.

6.8.10 Resistance temperature characteristic. The resistance temperature characteristics is the relationship between the zero power resistance of a thermistor and its body temperature (see 3.1).

6.8.11 Temperature wattage characteristic. The temperature wattage characteristic of a thermistor is the relationship at a specified ambient temperature between the thermistor temperature and the applied steady state wattage.

6.8.12 Current time characteristic. The current time characteristic is the relationship at a specified ambient temperature between the current through a thermistor and time, upon application or interruption of voltage to it.

6.8.13 Stability. The stability of a thermistor is the ability of a thermistor to retain specified characteristics after being to designated environment or electrical test conditions.

6.9 Subject term (key word) listing.

Coefficient, negative temperature
Coefficient, positive temperature
Dissipation constant
Thermal time constant
Zero power resistance

6.10 Amendment notations. The margins of this specification are marked with an asterisk to indicate modifications generated by this amendment. This was done as a convenience only and the Government assumes no liability whatsoever for any inaccuracies in these notations. Bidders and contractors are cautioned to evaluate the requirements of this document based on the entire content irrespective of the marginal notations.

APPENDIX A

PROCEDURE FOR QUALIFICATION INSPECTION

A.1 SCOPE

A.1.1 Scope. This appendix details the procedure for submission of samples for qualification inspection of thermistors covered by this specification. The procedure for extending qualification of the required sample to other thermistors covered by this specification is also outlined herein. This is a mandatory part of the specification. The information contained herein is intended for compliance.

A.2 APPLICABLE DOCUMENTS

A.2.1 General. The documents listed in this section are specified in sections A.3 and A.4 of this specification. This section does not include documents cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document user are cautioned that they meet all specified requirements documents cited in sections A.3 and A.4 of this specification, whether or not they are listed.

A.2.2 Government.

A.2.2.1 Specifications, standards, or handbooks. The following specifications, standards, or handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-1276 - Leads for Electronic Component Parts.

* (Copies of these documents are available online at https://quicksearch.dla.mil/.)

A.2.3 Order of precedence. Unless otherwise noted herein or in the contract, in the event of a conflict between the text of this document and the references cited herein (except for related, specification sheets), the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

A.3 SUBMISSION

A.3.1 Sample. A sample consisting of 62 units, 31 of the lowest and highest resistance values in each resistance ratio characteristic, and 31 of the lowest (tightest) resistance tolerance in each style for which qualification is sought shall be submitted. (For the solderability test, if both leads are tested, use 74 sample units. However, if one lead is to be tested, use 86 sample units.) Units for solderability test can be of any resistance value.

APPENDIX A

A.4 EXTENT OF QUALIFICATION

A.4.1 Extent of qualification. The extent of qualification between styles, terminations, and tolerances shall be as specified in table A-I.

TABLE A-I. Extension of qualification.

Style	Will qualify style 1 /
RCTP0303	RCTP0303
RCTN0404	RCTN0404
RCTP0805	RCTP0805
RCTN0805	RCTN0805, RCTN1206

Termination	Will qualify termination	May qualify termination with minor additional testing 2/
G	G	B, W
W	W	
B	B	G, W, C, U, S 3/
U	U, T	C, D
T	T	D
C	C, D	U, T
D	D	T
S	S	W

Resistance tolerance	Will qualify resistance tolerance
1.0	1.0, 2.0, 5.0, 10.0
2.0	2.0, 5.0, 10.0
5.0	5.0, 10.0
10.0	10.0

1/ The same design and technology must be utilized for the style qualified and the styles that the qualification is extended to.
2/ To be determined by qualifying activity.
3/ Must contain barrier layer to qualify.

Custodians:
Army – CR
Navy – EC
Air Force – 85
DLA - CC

Preparing activity:
DLA – CC

(Project 5905-2022-023)

Review activities:
Army – AT, AV, CR4
Navy – AS, CG, MC, OS
Air Force – 19

Civil agencies:
NASA – NA

NOTE: The activities listed above were interested in this document as of the date of this document. Since organizations and responsibilities can change, you should verify the currency of the information above using the ASSIST Online database at https://assist.dla.mil.